Ultra-Low Phase Noise 100 MHz Crystal Oscillator

Luke Dummott, Jeremy Everard, Simon Bale, St. John Gilbert

University of York, York, UK

Email: luke.dummott@york.ac.uk

This paper describes an ultra-low phase noise 100 MHz crystal oscillator that exhibits around -140 dBc/Hz at a 100 Hz offset. The constituent parts of the oscillator will be explained in detail and include a low noise parallel differential amplifier and digitally-controlled phase shifter and attenuator elements, which allow for a flexible approach in producing oscillators using alternative amplifiers and at different frequencies. The effects of using attenuation in the oscillator loop to improve phase noise is also explored. This builds on previous work on 10 MHz crystal oscillators[1].

The oscillator is made up of various elements as shown in Fig 1, each of which will be described in detail in the conference paper. The amplifier used is based around 4 long-tailed pair differential amplifiers in a parallel configuration that enables a higher maximum output power without introducing as much excess gain as would result from a single long-tailed pair operating at a similar power level. The digitally-controlled phase shifter and attenuator have been designed as a convenient way to set the loop power and phase, enabling quick comparisons of oscillator performance using different amplifiers and operating conditions. To minimise potential flicker noise, these are passive devices that use latching RF relays to switch microstrip delay lines / resistive attenuation networks into the signal path. As will be explored in the conference paper, the placement of the attenuator can also help to mitigate against sensitivity of the amplifier's noise performance to its source impedance and to maintain an optimal[2] Q_L/Q_0 in situations where the amplifier input impedance is not 50 Ω.

A measurement of the oscillator phase noise using the R&S FSWP is shown in Fig 2 with the listed data points ignoring spurious frequencies. It can be seen that a noise performance of -140 dBc/Hz at around a 100 Hz offset and a noise floor of -168 dBc/Hz has been achieved. Sponsors:- Keysight & EPSRC.

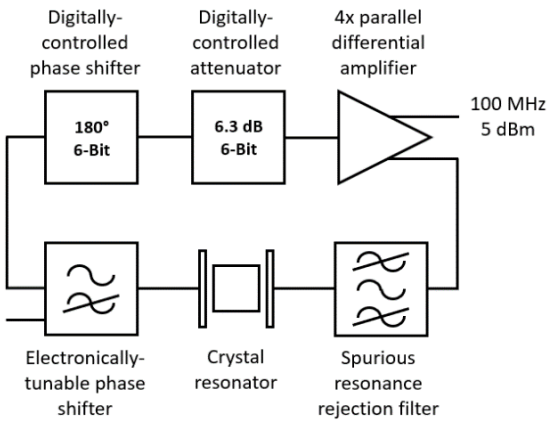

Fig 1: Oscillator block diagram

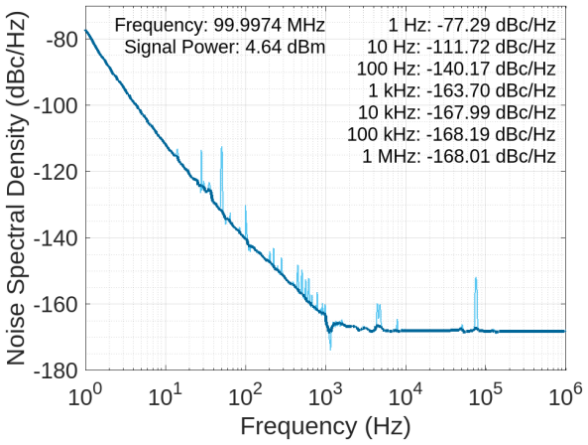

Fig 2: Phase noise measurement

[1] J. Everard, T. Burtichelov, and K. Ng, "Ultralow Phase Noise 10-MHz Crystal Oscillators", IEEE Trans. Ultrasonics, Ferroelectrics and Freq. Control, vol. 66, no. 1, January 2019

[2] J. Everard, "Fundamentals of RF Circuit Design with Low Noise Oscillators", ISBN: 0-471-49793-2, Wiley, Dec. 2000 reprinted Oct. 2002.